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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/943,238	10/01/97	HIROKI M	0756-1724

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EXAMINER	
RAO,S	
ART UNIT	**PAPER NUMBER**
2814	8

DATE MAILED: 08/31/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/943,238	Masaaki, Hiroki
Examiner	**Group Art Unit**
Steven Rao	2814

☒ Responsive to communication(s) filed on *Apr 26, 1999* .

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *21-40* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *21-40* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☒ The drawing(s) filed on *Oct 3, 1997* is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☒ received in Application No. (Series Code/Serial Number) *07/837,394* .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Drawings

1. The drawings in this application are objected to by the Draftsperson as informal. Any drawing corrections requested, but not made in the prior application should be repeated in this application if such changes are still desired. If the drawings were changed and approved during the prosecution of the prior application, a petition may be filed under 37 CFR 1.182 requesting the transfer of such drawings, provided the parent application has been abandoned. However, a copy of the drawings as originally filed must be included in the 37 CFR 1.60 application papers to indicate the original content.

2. This application, filed under former 37 CFR 1.60, lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

3. Figures 2 and 20 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The following title is suggested: "Method of Making an Active -type LCD with digitally graded display."

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are:

8. The disclosure is objected to because of the following informalities: .

a) Numerous parts identified by reference numerals in the drawings are not identified/described in the specification.

b) The specification fails to include line numbers throughout the specification.

c) The specification needs to be presented in an logical fashion wherein all the necessary steps for a particular embodiment need to be described in the order they are undertaken. Presently

the entire specification is a hodge podge of steps that are undertaken in several embodiments, and bits and parts of different embodiments are mixed together .

d) The specification appears to be a literal translation of a foreign language application/patent. The specification contains TOO Many grammatical and other errors to list all of them here.

Applicants' cooperation is sought to provide a substituted/amended specification without the numerous errors. Appropriate correction is required.

Claim Rejections - 35 U.S.C. § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (U.S. Patent No. 4,960,719 herein after Tanaka et al.) , and further in view of Aoyama et al. (Japanese Patent No. 62-283664, herein after Aoyama et al.) and Kishita et al. (U.S. Patent No. 4,650,543 herein after Kishita et al.).

Tanaka et al. discloses a method of producing an amorphous silicon thin film transistor array substrate including the steps of:

a) forming a gate electrode on an insulating surface of a substrate.

b) forming a gate insulating film over the gate electrode.

c) depositing an amorphous silicon semiconductor film on the gate insulating film.

d) depositing a n-type semiconductor layer on the amorphous semiconductor film by plasma CVD.

e) patterning the n-type semiconductor layer into source and drain regions.

f) forming an film over the n-type semiconductor layer after the above patterning step.

g) forming a pixel electrode over the film . (See Tanaka et al. Figs. 8a-8d and Column 4, lines 15-Column 5, line 55).

A. However Tanaka et al. does not specifically identify that one of the several ways of performing the disclosed plasma CVD as being carried out in the presence of a mixture of silane, phosphine and hydrogen. Aoyama et al. discloses the manufacture of thin film semiconductor device wherein a fine crystal and amorphous silicon are deposited by plasma CVD in a monosilane gas admixed with hydrogen and phosphine. As both Tanaka et al. and Aoyama et al. disclose the manufacture of TFTs having increased response speeds, it would have been obvious to one skilled in the art at the time the invention was made to use Aoyama et al's gas atmosphere (namely a mixture of Silane, Hydrogen & Phosphine) to carry out Tanaka et al.'s plasma CVD

method steps. Further using polyimide as leveling film is well known in the art. Eg. Kitazima et al. (Col.4, lines 50-52).

B. With respect to claims 22 and 23 the selection of a desired temperature range and r.f power are merely the choosing of desired parameters, which without recited criticality or unexpected results, etc. does not patentably distinguish over the cited prior art.

C. With respect to claim 24, Kishita et al. discloses gate electrodes of doped silicon film and molybdenum film thereon. (See Col. 2).

D. With respect to claim 25, it is well known in the art to form Aluminum gate electrode. Eg. Applicants' cited prior art namely Japanese Patent No.: 156725. Further Kishita et al. discloses that Au or Al can be interchangeably used for gate electrodes (Col.2, lines 53-57).

E. With respect to claim 26, Tanaka et al. discloses in Column 1, lines 64-66 a gate insulating layer (film) 23 of silicon nitride or silicon oxide.

F. With respect to claim 27, Tanaka et al. discloses at Col.4, lines 32-36 that silicon oxide insulating layer is treated with a buffer fluoric acid solution. Applicants' listed prior art, namely U.S. Patent No.: 4,949,141 (Busta) in Col.4, lines 60-65 state the use of fluorine etc.

G. With respect to claim 28, Tanaka et al. discloses in Column 2, lines 1-5 that the amorphous semiconductor film is deposited through plasma CVD.

H. With respect to claim 28, it is well known in the art to produce a amorphous semiconductor film of 500 to 5000^{0} A. Eg. Wolf Vol. 1, pages 191-195. Further mere selection of a desired range of film thickness does not patentably distinguish the claim over the cited prior art.

I. With respect to claim 30, as stated above Aoyama et al. discloses the use of monosilanes.

J. With respect to claim 31, Tanaka et al. discloses an organic layer in direct contact with the semiconductor film. Also see Applicants' listed prior art, namely U.S. Patent No. 5,084,905, Figure 10 F.

K. With respect to claim 32, it includes subject matter of claims 21 and 30 and therefore claim 32 is rejected for reasons recited in claims 21 and 30 above.

L. With respect to claim 33, it is well known in the art to have a n-type semiconductor layer with different conductivities and merely choosing the desired range of conductivity namely 2 x 10^{1} ( ). Does not patentably distinguish it over the cited prior art.

M. With respect to claim 34, it repeats subject matter of claim 31 and therefore is rejected for reasons set out in claim 31 above.

N. With respect to claim 35, it recites the subject matter in claims 21 and 31 wherein the source and drain regions and electrodes are similarly patterned. In addition to the reasons recited under claims 21 and 31 above, Applicants' listed prior art U.S. Patent No. : 5,084,904 Sasaki et al. in figures 9 and 10F disclose similarly patterned source & drain regions and electrodes.

O. With respect to claims 36 and 38 they are rejected for reasons set out under Claim 30 above.

P. With respect to claim 37 it recites subject matter covered by claim 21 and additionally having the pixel electrode extending over the channel region. In addition to the rejections under claim 21 above, Applicants' listed prior art U.S. Patent No. 5,084,904 Sasaki et al. In figures 9 and 10F discloses pixel electrodes extending over the channel region.

Q. With respect to claim 39, it is rejected for reasons set out under claim 31 above.

R. With respect to claim 40, it recites subject matter covered by claims 35 or 37 and additionally recites that the inner edges of the source and drain regions are aligned with the inner edges of the source and drain electrodes. In addition to the rejections under claims 35 or 37 above, Applicants' listed prior art U.S. Patent No. : 5,084,904 Sasaki et al. in figures 9 and 10F discloses that the inner edges of the source and drain regions are aligned with the inner edges of the source and drain electrodes.

7. The prior art made of record and not relied upon in this office action but is considered pertinent to applicant's disclosure are: a) G.B. Patent No. 2,187,859 which disclose a method of producing liquid crystal devices.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The

fax number is (703) 308-7722 or -7724.The Examiner can be normally reached on Monday-Friday from 9.30 a.m. to 6.00 p.m. (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor Ex. Olik Chaudhuri, can be reached at (703) 306-2794.

9. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission at the above mentioned fax numbers.

10. Any inquiry of a general nature or relating to the status of this application should be directed to the Technology center 2800 receptionist at (703) 308-0956.

Aug. 30 1999.

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800